AMENDMENTS TO THE CLAIMS:

Please replace the claims with the claims provided in the listing below wherein status, amendments, additions and cancellations are indicated.

1. (Currently Amended) A re-programmable logic integrated circuit ~~such as a field programmable gate array having a CPU core~~ , comprising:

a ~~wherein the~~ CPU core [[is]] provided with registers, memories and a controller for the registers and memories;

~~wherein~~ the CPU core [[has]] having instructions including microcode; and

~~wherein~~ the controller [[has]] having control lines for outputting enable signals to the registers and memories, the controller reading ~~reads~~ in [[the]] an instruction of the instructions, and ~~transmits~~ transmitting ON/OFF information for each of bits composing the microcode included in the instruction to ones of the registers and memories allocated to each of the bits, thereby controlling the registers and memories through the directing control lines

wherein the CPU core has address pointer registers used in accessing the memories;

wherein the controller has directing control lines for giving either direction of increment and decrement to the address pointer registers, reads in the

instructions, and transmits ON/OFF information for each of bits for giving either direction of increment and decrement to the address pointer registers in microcode included in the instruction through the directing control lines; and

wherein the address pointer registers counts up or counts down values of maintaining addresses when receiving ON information about the bits for giving either direction of increment and decrement from the controller through the directing control lines.

2. (Canceled)

3. (Original) The logic integrated circuit according to claim 1, wherein the CPU core is further provided with general-purpose registers, and a data transmitting path for connecting the general-purpose registers and memories only through multiplexers for inputting and outputting to and from the general-purpose registers without passing through multiplexers for inputting and outputting memory data, and wherein the CPU core inputs data from the memories to the general-purpose registers with using the data transmitting path.

4. (Original) The logic integrated circuit according to claim 1, wherein the CPU core is further provided with general-purpose registers, and a data

transmitting path for connecting the general-purpose registers and memories only through multiplexers for inputting and outputting to and from the general-purpose registers without passing through ALU, and wherein the CPU core outputs data to the memories with using the data transmitting path.

5. (Original) The logic integrated circuit according to claim 1, wherein the CPU core comprises multiplexers including an integrated interface for inputting data from FIFO that is an accessible memory having data input and output units which are separated from each other, and wherein the CPU core has instructions for reading in data from the FIFO through the multiplexers.

6. (Currently Amended) A recording medium which is capable of being read out by computers, and records executable code ~~a source as~~ including circuit information for ~~composing a~~ implementing the CPU core of claim 1 in the re-programmable logic integrated circuit, the executable code being based on ~~wherein the source is described at~~ hardware description language level for the CPU core ~~on the logic integrated circuit described in claim 1~~.

7-11. (Canceled)

12. (New) The re-programmable logic circuit of claim 1 wherein the re-programmable logic circuit is a field programmable gate array.

13. (New) The re-programmable logic circuit of claim 3 wherein the re-programmable logic circuit is a field programmable gate array.

14. (New) The re-programmable logic circuit of claim 4 wherein the re-programmable logic circuit is a field programmable gate array.

15. (New) The re-programmable logic circuit of claim 5 wherein the re-programmable logic circuit is a field programmable gate array.

16. (New) The recording medium of claim 6 wherein the re-programmable logic circuit is a field programmable gate array.